Application Analysis Tools For Asip Design Application Profiling And Instruction Set Customization 1

Hardware-dependent SoftwareIEEE International High-Level Design Validation and Test WorkshopProceedings of the International Symposium on Hardware/Software CodesignProceedingsCustomizable Embedded ProcessorsProceedings of the FAA-NASA Symposium on the Continued Airworthiness of Aircraft StructuresProceedings, International Symposium on VLSI DesignACM SIGPLAN NoticesEmbedded DSP Processor DesignXIII SBMicro, International Conference on Microelectronics and Packaging, ICMP'98: Advanced courses and invited papersProceedingsMaterials and Process ChallengesAerospace EngineeringProceedings of the Seventh International Symposium on High-level SynthesisProceedingsProceedingsDissertation Abstracts InternationalCODES 2002Building ASIPs: The Mescal MethodologyJournal of Information Science and EngineeringCASES 2003Ship Structure Committee PublicationsAcronyms, Initialisms & Abbreviations DictionaryCODES+ISSS EUROMICRO 97, Proceedings of the 23rd EUROMICRO ConferenceStructure-Oriented EvaluationProceedings of the ACM Great Lakes Symposium on VLSI.Energy-Efficient Communication ProcessorsIEEE/ACM International Conference on Computer Aided DesignA RAND Analysis Tool for Intelligence, Surveillance, and Reconnaissance1997 Design Automation ConferenceHardware/Software Co-DesignCASES Proceedings of Technical PapersLanguage-driven Exploration and Implementation of Partially Re-configurable ASIPsProceedings of the Third International Conference on Knowledge Discovery and Data MiningTIPIEDN, Electrical Design NewsApplication Analysis Tools for ASIP DesignIssues in Electronic Circuits, Devices, and Materials: 2011 Edition

Hardware-dependent Software

IEEE International High-Level Design Validation and Test Workshop

Proceedings of the International Symposium on Hardware/Software Codesign

Proceedings

Customizable Embedded Processors

Proceedings of the FAA-NASA Symposium on the Continued Airworthiness of Aircraft Structures

Proceedings, International Symposium on VLSI Design

ACM SIGPLAN Notices

Embedded DSP Processor Design

Customizable processors have been described as the next natural step in the evolution of the microprocessor business: a step in the life of a new technology where top performance alone is no longer sufficient to guarantee market success. Other factors become fundamental, such as time to market, convenience, energy efficiency, and ease of customization. This book is the first to explore comprehensively one of the most fundamental trends which emerged in the last decade: to treat processors not as rigid, fixed entities, which designers include “as is in their products; but rather, to build sound methodologies to tailor-fit processors to the specific needs of such products. This book addresses the goal of maintaining a very large family of processors, with a wide range of features, at a cost comparable to that of maintaining a single processor. First book to present comprehensively the major ASIP design methodologies and tools without any particular bias Written by most of the pioneers and top international experts of this young domain Unique mix of management perspective, technical detail, research outlook, and practical implementation

XIII SBMicro, International Conference on Microelectronics and Packaging, ICMP'98: Advanced courses and invited papers

Proceedings

Concurrent design, or co-design of hardware and software is extremely important for meeting design goals, such as high performance, that are the key to commercial competitiveness. Hardware/Software Co-Design covers many aspects of the subject, including methods and examples for designing: (1) general purpose and embedded computing systems based on instruction set processors; (2) telecommunication systems using general purpose digital signal processors as well as application specific instruction set processors; (3) embedded control systems and applications to automotive electronics. The book also surveys the areas of emulation and prototyping systems with field programmable gate array technologies, hardware/software synthesis and verification, and industrial design trends. Most contributions emphasize the design methodology, the requirements and state of the art of computer aided co-design tools, together with current design examples.

Materials and Process Challenges

Aerospace Engineering

Proceedings of the Seventh International Symposium on High-level Synthesis

Despite its importance, the role of HdS is most often underestimated and the topic is not well represented in literature and education. To address this, Hardware-dependent Software brings together experts from different HdS areas. By providing a comprehensive overview of general HdS principles, tools, and applications, this book provides adequate insight into the current technology and upcoming developments in the domain of HdS. The reader will find an interesting text book with self-contained introductions to the principles of Real-Time Operating Systems (RTOS), the emerging BIOS successor UEFI, and the Hardware Abstraction Layer (HAL). Other chapters cover industrial applications, verification, and tool environments. Tool introductions cover the application of tools in the ASIP software tool chain (i.e. Tensilica) and the generation of drivers and OS components from C-based languages. Applications focus on telecommunication and automotive systems.

Proceedings

The RAND Corporation's Collection Operations Model (COM) is a stochastic, agent-based simulation tool designed to support the analysis of command, control, communications, intelligence, surveillance, and reconnaissance (C3ISR) processes and scenarios. Written for the System Effectiveness Analysis Simulation modeling environment, the COM is used to study processes that require the real-time interaction of many players and to answer questions about force mix, system effectiveness, concepts of operations, basing and logistics, and capability-based assessment. It can represent thousands of autonomous, interacting platforms and explore the capabilities of a wide range of intelligence, surveillance, and reconnaissance assets. Through its flexible and friendly text-based input tables, the model represents a wide array of sensor capabilities, target properties, terrain and weather effects, and resource limitations. Its final output is a minute-by-minute account of each agent's changing operational picture. Since 2005, the COM has been used to model counterinsurgency, counterpiracy, and maritime surveillance scenarios and two major combat operations, and to study ad hoc collections, sensor cueing, dynamic retasking, and resource allocation. RAND has planned a number of upgrades to the COM, including the addition of space-based assets; a more robust model of sensor data fusion; communications modules that more accurately represent the advantages of a networked force; a more realistic representation of C3ISR workflow; sensor capability to generate false positives; and agent capability to practice deception. These extensions and enhancements are intended to result in a COM that can represent the entire C3ISR process specifically and network-centric operations in general.

Proceedings

Issues in Electronic Circuits, Devices, and Materials: 2011 Edition is a

ScholarlyEditions™ eBook that delivers timely, authoritative, and comprehensive information about Electronic Circuits, Devices, and Materials. The editors have built Issues in Electronic Circuits, Devices, and Materials: 2011 Edition on the vast information databases of ScholarlyNews.™ You can expect the information about Electronic Circuits, Devices, and Materials in this eBook to be deeper than what you can access anywhere else, as well as consistently reliable, authoritative, informed, and relevant. The content of Issues in Electronic Circuits, Devices, and Materials: 2011 Edition has been produced by the world's leading scientists, engineers, analysts, research institutions, and companies. All of the content is from peer-reviewed sources, and all of it is written, assembled, and edited by the editors at ScholarlyEditions™ and available exclusively from us. You now have a source you can cite with authority, confidence, and credibility. More information is available at http://www.ScholarlyEditions.com/.

Dissertation Abstracts International

CODES 2002

Building ASIPs: The Mescal Methodology

Journal of Information Science and Engineering

CASES 2003

Ship Structure Committee Publications

Acronyms, Initialisms & Abbreviations Dictionary

CODES+ISSS

EUROMICRO 97, Proceedings of the 23rd EUROMICRO Conference

This book introduces a new branch of evaluation theory, where evaluation and score calculation is embedded into general measure theory, as is typical in geometry, probability theory and reliability theory. The author describes the theoretical background of new evaluation model for complex processes, where interests of involved groups are considered as multi-players of evaluation process. Readers will learn how the logical structure of a process/system can be included into an evaluation. The author applies these techniques not only to the

visualization of evaluation goals, but also the designed logical structure becomes the basis for calculation of evaluation scores. Various examples are provides to demonstrate the implementation of the methods.

Structure-Oriented Evaluation

Proceedings of the ACM Great Lakes Symposium on VLSI.

Hot topics discussed in these March 1997 proceedings include networked CAD systems, deep submicron CAD, and multichip packages for consumer applications. The other 114 papers were presented in sessions such as sequential ATPG; design for analog circuits; advances in build-in self test; synthesis of controllers; microsystems design; software generation for embedded processors; register transfer level test synthesis; BDDs and formal verification; high performance architectures for multimedia and communication ASICs; decision diagrams and diagnosis; performance modeling; progress in IDDQ test technology; architecture exploration; layout design; and power modeling and estimation. No index. Annotation copyrighted by Book News, Inc., Portland, OR.

Energy-Efficient Communication Processors

An increasing number of system designers are using ASIP’s rather than ASIC’s to implement their system solutions. Building ASIPs: The Mescal Methodology gives a simple but comprehensive methodology for the design of these application-specific instruction processors (ASIPs). The key elements of this methodology are: Judiciously using benchmarking Inclusively identifying the architectural space Efficiently describing and evaluating the ASIPs Comprehensively exploring the design space Successfully deploying the ASIP This book includes demonstrations of applications of the methodologies using the Tipi research framework as well as state-of-the-art commercial toolsets from CoWare and Tensilica.

IEEE/ACM International Conference on Computer Aided Design

A RAND Analysis Tool for Intelligence, Surveillance, and Reconnaissance

1997 Design Automation Conference

This book introduces a novel design methodology which can significantly reduce the ASIP development effort through high degrees of design automation. The key elements of this new design methodology are a powerful application profiler and an automated instruction-set customization tool which considerably lighten the burden of mapping a target application to an ASIP architecture in the initial design stages. The book includes several design case studies with real life embedded applications to demonstrate how the methodology and the tools can be used in practice for accelerating the overall ASIP design process.

Hardware/Software Co-Design

CASES

Proceedings of Technical Papers

This book provides design methods for Digital Signal Processors and Application Specific Instruction set Processors, based on the author's extensive, industrial design experience. Top-down and bottom-up design methodologies are presented, providing valuable guidance for both students and practicing design engineers. Coverage includes design of internal-external data types, application specific instruction sets, micro architectures, including designs for datapath and control path, as well as memory sub systems. Integration and verification of a DSP-ASIP processor are discussed and reinforced with extensive examples. Instruction set design for application specific processors based on fast application profiling Micro architecture design methodology Micro architecture design details based on real examples Extendable architecture design protocols Design for efficient memory sub systems (minimizing on chip memory and cost) Real example designs based on extensive, industrial experiences

Language-driven Exploration and Implementation of Partially Re-configurable ASIPs

Proceedings of the Third International Conference on Knowledge Discovery and Data Mining

AAAI proceedings describe innovative concepts, techniques, perspectives, and observations that present promising research directions in artificial intelligence.

TIPI

This volume contains papers presented at the 23rd Euromicro Conference on New Frontiers of Information Technology.

EDN, Electrical Design News

This book describes a new design approach for energy-efficient, Domain-Specific Instruction set Processor (DSIP) architectures for the wireless baseband domain. The innovative techniques presented enable co-design of algorithms, architectures and technology, for efficient implementation of the most advanced technologies. To demonstrate the feasibility of the author’s design approach, case studies are included for crucial functionality of advanced wireless systems with increased computational performance, flexibility and reusability. Designers using this approach will benefit from reduced development/product costs and greater scalability to future process technology nodes.

Application Analysis Tools for ASIP Design

Increasing complexity of modern embedded systems demands system designers to ramp up their design productivity without compromising performance goals. This is promoted by modern Electronic System Level (ESL) techniques. Language-driven Exploration and Implementation of Partially Re-configurable ASIPs addresses an important segment of the ESL area by modeling partially re-configurable processors via high-level Architecture Description Language (ADL). This approach also hints an imminent evolution in the area of re-configurable system design.

Issues in Electronic Circuits, Devices, and Materials: 2011 Edition